Q1) 0 DRC violations are reported,

the total area of the top module in square micron is 258.115 square micron, the total power of the design in 2.33769348 milliwatt

the slack in nanoseconds after placement and routing is 0.031

Q2) The smallest die area you can get without getting any DRC violations is 266.5624 square micron

Q3)

The total area remain unchange ,but the slack will decrease. The reason is the higher row density can lead to shorter delay.

Q4)

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